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A design-based approach to planarization in multilayer surface micromachining

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Abstract. This paper describes a design-based planarization strategy that can control topography to within submicron levels. The design concept takes advantage of the inherent conformability of the film deposition processes to achieve planar topography, without the need for an additional planarization step. It is based on a universally regulating line spacing in patterned layers to within a predefined amount, thus allowing subsequent layers to fill in as they grow, conforming to the previous layer. Test structures were fabricated to study the effect of different feature sizes in underlying layers on the topography of subsequent layers. Predictions based on numerical and geometric models for topography generation are compared to fabricated devices. An example of successful application to a micromachined adaptive mirror is presented.

1. Introduction

Multiple layer thin-film processes result in structures with a large surface topography due to the conformal nature of film growth. Typically, in surface micromachining, each patterned layer adds to subsequent layers topography variations of a magnitude equal to its own thickness. This introduces several problems in the processing of subsequent layers related to step coverage during photoresist spinning, the depth of focus of the lithography system and the formation of stringers during reactive ion etching. Planarization has thus been a long-standing issue, and is a key manufacturing step in the integrated circuit (IC) industry, particularly in the fabrication of multi-level metal interconnects used in high-density ICs. The IC industry formerly used several methods such as borophosphosilicate glass (BPSG) reflow [1], spin-on-glass [2], and plasma etching [3] to achieve planarization. Subsequently, chemical–mechanical polishing (CMP) emerged as a powerful technology for global planarization of ICs. CMP is now an established technology for polishing polycrystalline silicon, as well as for planarization of silicon dioxide, which is the interlevel dielectric. In the latter case, sacrificial oxide layers are planarized by rotating a wafer under pressure against a polishing pad in the presence of a silica-based alkaline slurry [4].

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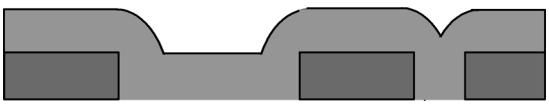

Figure 1. A large gap between two features on the lower layer (dark gray) results in topography in the upper layer (light gray) equal to the thickness of the lower layer, whereas a small gap results in much smaller topography.

More recently, planarization issues have become prominent in the microelectromechanical systems (MEMS) industry. In the fabrication of most MEMS devices, relatively thick (2 μm or greater) layers are grown and patterned, generating large surface topography. In addition to the processing issues described above, MEMS devices often require planar surfaces for functional reasons. Unlike ICs, many MEMS devices (such as micro-engines, linkages and gears) have meshing, moving parts, and planar surfaces are clearly important for such structures. Similarly, surface planarity and roughness are of crucial interest for optical MEMS devices. MEMS researchers have demonstrated success with local planarization techniques for some sensor applications [5, 6]. The challenge in using CMP for MEMS is that structures with multiple structural levels often have several micrometers of built-up topography. Nevertheless, CMP has also been applied with remarkable success to MEMS devices [7, 8].

We have developed a unique approach to planarization that can be used as a stand-alone scheme or in conjunction

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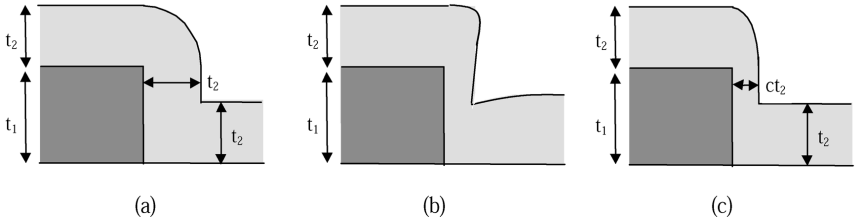

Figure 2. Illustration of film growth at a step, as a function of c.

with CMP. The planarization strategy described in this paper evolved as part of a research effort to develop surface-micromachined, continuous and segmented deformable mirrors controlled by an array of surface normal electrostatic actuators [9, 10]. Silicon-based microsystem components are well suited to opto-mechanical applications. However, built-up topography in the optical layer is a prominent design and fabrication issue in optical applications requiring smooth surfaces.

2. Planarization strategy

The planarization design concept is based on the idea that a small enough gap between two features on a layer will get filled in by the succeeding layer(s). Figure 1 illustrates this idea. It is easy to see that as more layers are deposited over the area on the right, the print-through to the upper layers will progressively diminish. By globally implementing this technique and using only very narrow cuts in all layers, it is possible to generate nominally planar topography. The conformal deposition processes in surface micromachining act to rapidly fill in cuts from previously deposited layers, largely limiting the magnitude of their 'print-through' to subsequent layers.

We used a polysilicon surface micromachining process with PSG (phosphosilicate glass) as the sacrificial material. For this process, 1.5 μm was selected as the maximum spacing between the features on any polysilicon layer and as the maximum width of anchor cuts in oxide layers. Larger areas, where polysilicon would normally have been removed, were instead left as isolated polysilicon islands, surrounded by a 1.5 μm wide trench-cut. Anchoring sites, which would be structurally weak if only 1.5 μm in width, were fabricated as honeycomb structures of thin polysilicon walls encapsulating a thicker structure of oxide, to provide sufficient structural strength.

3. Topography generation models

Chemical vapor deposition (CVD) is the most popular technique used to deposit thin films in surface micromachining processes, since it affords excellent control over film growth and step coverage. CVD is a complicated process involving diffusion of the reactant gases to the surface, adsorption onto the surface, surface diffusion and reaction, desorption of the product gases and diffusion of the products away from the surface. The film grows on the side walls of features and not just along line of sight, thus resulting in uniform layer coverage of multistep topography. CVD processes have been extensively studied and modeled to understand the complicated chemistry and physics involved. Rarefied gas transport is usually considered in the modeling of CVD processes, since

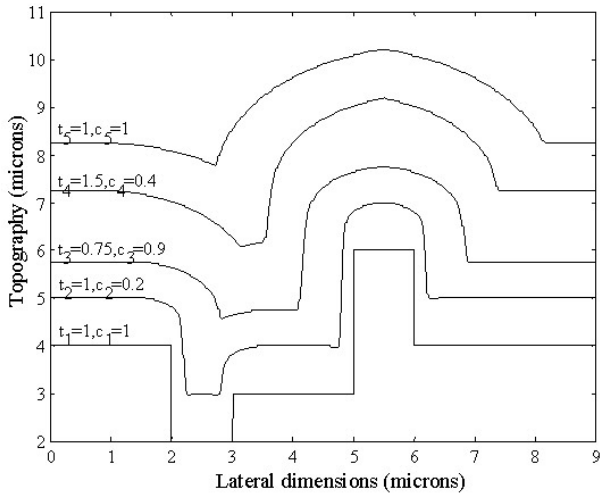

Figure 3. Numerically generated film profiles for an arbitrary starting topography.

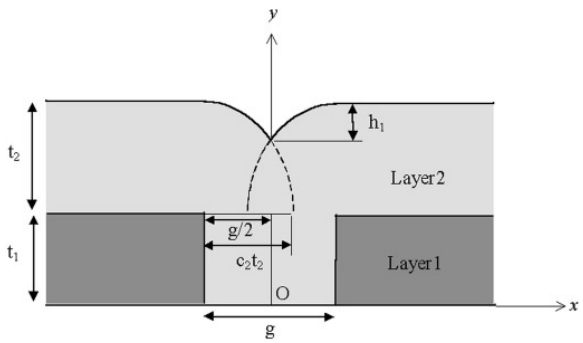

Figure 4. Topography generation over a gap g when a partially conformal film is deposited.

the mean free path of the molecules is less than feature size. Other things that are taken into account are the surface reaction probability of molecules and surface diffusion (usually described by a reactive sticking coefficient). Extensive research has been conducted to describe film profile evolution and microstructure formation, particularly in narrow trenches and contact vias [11–14]. Profile simulation approaches typically include string algorithms or particle pile-up methods.

We describe two-dimensional models to generate film profiles in infinitely-long trenches. These models are based on a purely geometrical approach, with a view to predicting topography generation for the planarization scheme described above.

Figure 2 illustrates the progression of conformal film growth at a step. In figure 2(a), the upper film is 100% conformal, and uniform step coverage is achieved. In this case at every point on the underlying surface the film grows at the same rate normal to the local tangent to the surface at that point. This results in the film thickness on the sidewall of the

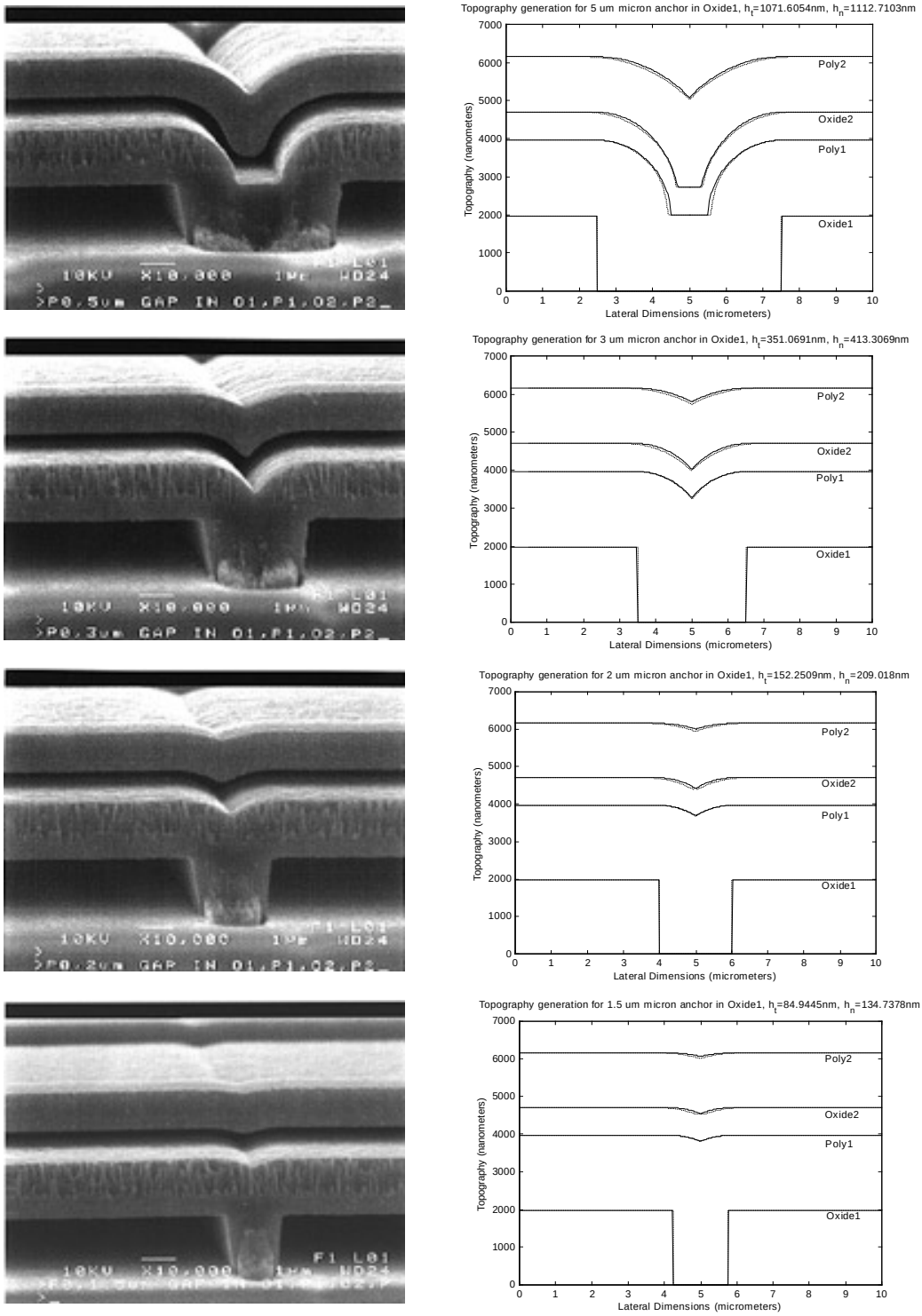

Figure 5. SEM micrographs (10 000 times magnification), geometric prediction (full curve) and numerical prediction (broken curve) for various trench widths in *Oxide1*.

step being equal to the vertical film thickness. CVD deposited polysilicon and silicon nitride are usually conformal as shown in figure 2(a) [15]. Figure 2(b) shows how shadowing effects from accumulated material in the corner causes non-conformal step coverage, as is often the case with silicon dioxide films. For the purposes of geometric modeling, we approximate this profile by assuming a uniform thickness along the sidewall, as shown in figure 2(c). We define a parameter c, which characterizes the extent of conformal deposition. This parameter defines the ratio of the film growth rate normal to the sidewall to the film growth rate in the vertical direction. In general, if a partially conformal film has a thickness of t in the vertical direction, it has a thickness of ct normal to the sidewall.

3.1. Numerical model

A numerical scheme was developed to generate film growth profiles for any arbitrary starting topography. The starting topography, such as a trench, is first discretized on a regular

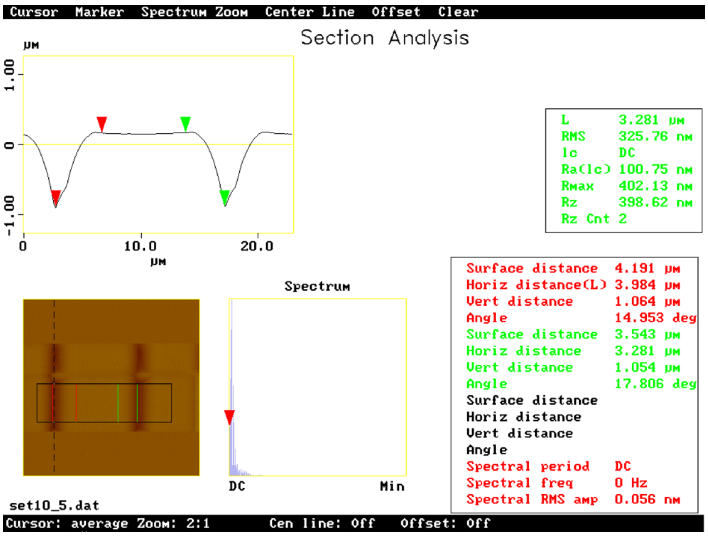

Figure 6. AFM scan across two topographical features in *Poly2* as a result of 5 μm wide gaps in *Oxide1*. The average step height is 1059 nm.

mesh. The local slope of each discrete element of this underlying topography is then calculated by using finite difference principles. Next, the film growth is simulated in a discrete fashion, the direction being normal to the local slope. The discrete film thickness is a function of the nominal film thickness, the conformability parameter c and the direction vector. The dependence of the local film thickness on the direction vector has been assumed to be linear. Figure 3 shows an example of conformal film growth simulated numerically for an arbitrary starting topography.

3.2. Geometric model

A two-dimensional geometric model was also developed to simulate the topography generation above an infinitely-long trench. For ease of implementation, the model assumes sharp corners and vertical side walls for all features created by reactive ion etching. This is a reasonable assumption except in the case of very thick layers where the side wall angle may become significant. Consider a case where there is a gap g between two features on layer 1, which has a thickness of t_1, as shown in figure 4. A film with thickness t_2 and index c_2 is deposited on top of this topography.

Using the frame of reference shown in figure 4, a second order polynomial can be used to describe the right half (corresponding to positive x-coordinates) of the curve

$$y_2 = t_1 + \left[t_2^2 - \frac{(x - (g/2))^2}{c_2^2} \right]^{1/2}. \qquad (1)$$

This equation is used to generate the topography of layer 2 for $0 < x < g/2$. For $-g/2 < x < 0$, the curve is symmetric about the y-axis. For all other values of x, $y = t_1 + t_2$. Note that (1) is valid for $c_2 \neq 0$ and $0 \leqslant g < 2ct_2$.

By extension, the topography of subsequent layers can be generated. In general, if there are N layers having thicknesses t_1–t_N and indices c_1–c_N, and there is a gap g on the first layer, the topography of the kth layer is given by

$$y_k = t_1 + \left[1 - \frac{(x - (g/2))^2}{(\sum_{n=2}^{k} c_n t_n)^2} \right]^{1/2} \sum_{n=2}^{k} t_n. \qquad (2)$$

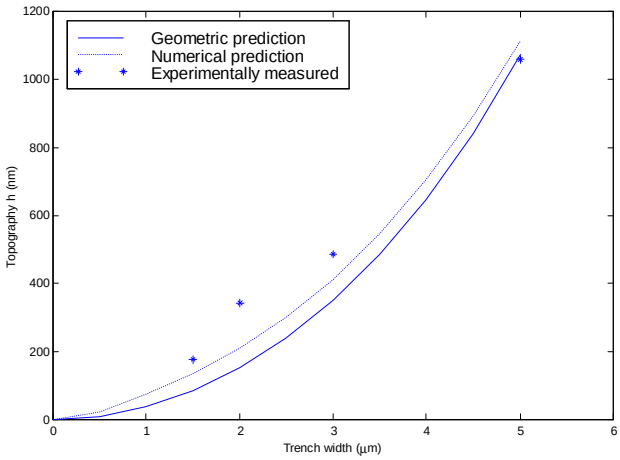

Figure 7. Comparison of experimentally measured topography with theoretical and numerically predicted topography.

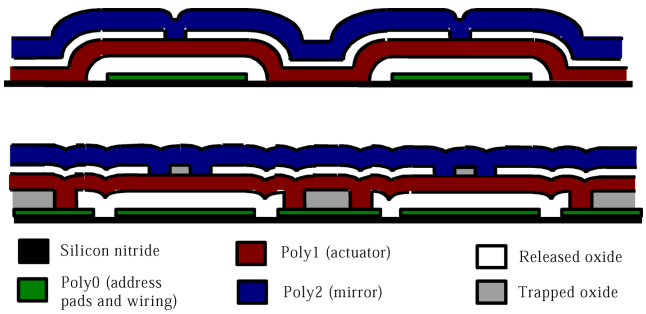

Figure 8. Illustration of conformal effects of deposition resulting in large topography for the deformable mirror, and relatively planar surfaces for narrow patterned features.

Again, (2) is valid for $\sum_{n=2}^{k} c_n t_n \neq 0$ and $g^2 \leqslant 4(\sum_{n=2}^{k} c_n t_n)^2$ or $g \leqslant 2(\sum_{n=2}^{k} c_n t_n)$.

4. Experimental results

Test structures were fabricated using the MCNC multi-user MEMS process (MUMPS), a three-layer polysilicon

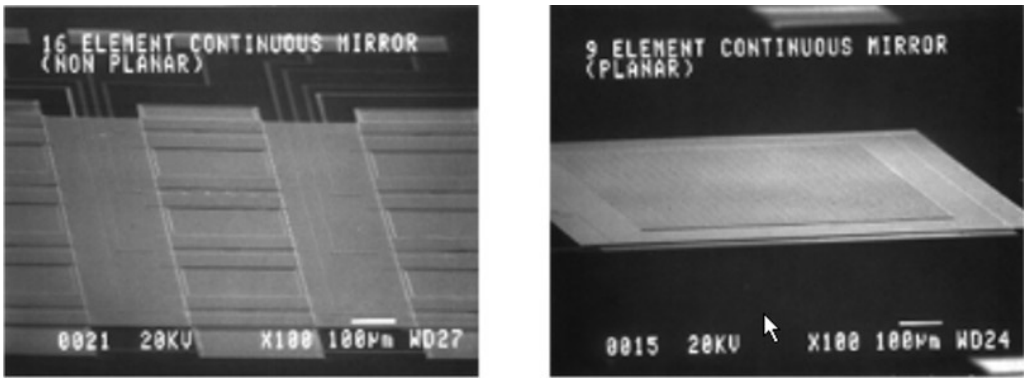

Figure 9. Planarization results for surface micromachined mirrors (SEM photos at 100 times magnification).

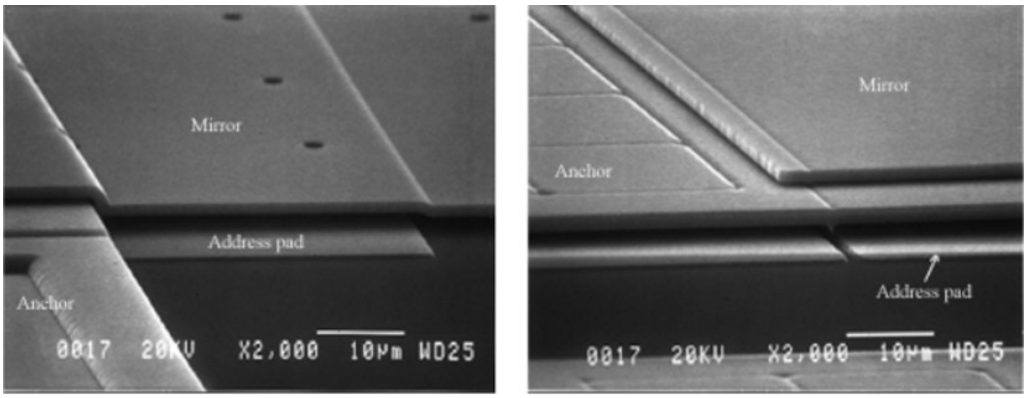

Figure 10. Planarization results for surface micromachined mirrors (SEM photos at magnification 10 000 times).

surface micromachining process [16]. Film thicknesses for polysilicon, PSG and silicon nitride were measured using a Leitz MPV-SP micro-spectrometer, while the film thickness of the metal layer was measured using a Dektak 3030 Profilometer. The test structures were fabricated in the MUMPS14 run, and the layers used were *Nitride* (581.9 nm), *Poly0* (506.0 nm), *Oxide1* (1971.3 nm), *Poly1* (1989.9 nm), *Oxide2* (734.4 nm), *Poly2* (1455.5 nm) and *Metal* (456.4 nm). These numbers are used in the topography generation models.

An example of the planarization models compared to fabricated devices is presented. The effect of varying trench width in the *Oxide1* film, which serves to anchor *Poly1* to the substrate, was studied. Figure 5 shows the scanning electron microscope (SEM) micrographs corresponding to the different gaps in *Oxide1*, with the corresponding topography generated by the models to the right of each micrograph. To generate this topography, a gap g was patterned into *Oxide1* and all the other films (*Poly1*, *Oxide2*, *Poly2*) were deposited without any patterning over the gap. The oxides were released using a hydrofluoric acid sacrificial etch.

We assume $c = 1$ for the polysilicon, since polysilicon is known to exhibit highly conformal growth. The conformability of *Oxide2* varies as a function of process conditions and the local geometry. For the MUMPs process, the step coverage over isolated lines or along the edge of large features is approximately 55%. On gratings or narrow gaps ($\sim 2\ \mu$m) the step coverage is only 35–40%. Thus, this is not a constant number and it varies as the growing films result in a narrower trench. The effect of varying c of the oxide layers on the topography was studied. In general, a 10% change in c led to a 1–2% change in h over the range of possible values for c. For the results presented, we assume a constant value of $c = 0.4$ for *Oxide2*.

In order to make quantitative assessments of computed and fabricated topography, high-resolution measurements of *Poly2* topography were made using an atomic force microscope (AFM) (Digital Instruments Dimension 3000 Scanning Probe Microscope) for all four cases. Figure 6 shows a typical AFM scan, indicating surface topography across two identical features. These correspond to the topography generated in the uppermost polysilicon (*Poly2*) layer as a result of 5 μm wide trenches in *Oxide1*. All measurements were made twice in this fashion and the average measured step heights were compared to the predicted step heights.

Figure 7 shows a comparison of the measured *Poly2* topography with the predictions. It is seen that the measured values differ from the predicted values by 5–50%. There are several sources of error in both the measured values as well as the models. It is possible that in the measurement, the scanning probe does not get to the very bottom of the crevice. At the same time, since the test structures were released, the probe could be pushing down on the structure and partially bending it. Both the geometric and numerical models make certain approximations as to the physical situation by assuming vertical sidewalls and sharp corners. The conformability parameter c is, at best, a rough approximation of the film growth on the sidewall. Other inaccuracies in the physical data include uncertainties in the film thicknesses and the starting step height. The numerical model, in addition to the above, has discretization and round-off errors. Both models could be improved by making better approximations of the physical situation.

The modeling approach is valid for a variety of processes and process flows. Since an empirical value is used for c, some information is required regarding the conformal step coverage of each layer.

5. Application

For our target application (deformable mirrors for adaptive optics), an optical quality surface is required. With a three-layer polysilicon process, we found that the final polysilicon layer had more than 5 μm of non-planarity as a result of patterning in the underlying layers. Figure 8 (top) is a schematic showing how topography might be cumulatively generated for the deformable mirror design, and how the new design concept can be utilized to alleviate this (bottom).

Qualitative examination using scanning electron microscopy indicates significant gains in surface planarity achieved through this technique. In figure 9, the SEM micrograph on the left is of a MEMS mirror supported on 16 cantilever actuators, fabricated using the MUMPS process without efforts towards planarization. The underlying features (electrostatic actuators and polysilicon electrodes) emboss the mirror membrane, leading to poor planarity. On the right-hand side is a MEMS mirror supported over a nine-element array of actuators. At this relatively low magnification, almost no print-through of the underlying structures is observed in the planarized structure. Figure 10 shows the two devices at a higher magnification. It is clearly seen that nominal planarization has been achieved, however there is some print-through of the narrow underlying gaps. In the next generation design, CMP can be included as a final planarization step to generate the optical surface. Several generations of continuous and segmented mirrors have been fabricated using this planarization approach. Results from prototype mirrors have been previously reported [17].

6. Conclusion

There exist technological challenges associated with CMP for step heights in the 2 μm or higher range. As thicker layers are used in multiple-layer processes for sophisticated MEMS devices, planarization will continue to be an important issue and an even greater challenge. The planarization approach presented in this paper could have wide-ranging applications in MEMS technology. The MUMPS process was used as a demonstration vehicle, and we have shown that it works well for this particular process. The approach is very generally applicable in all planarization situations where the film growth is conformal. This approach is not limited by the thickness of the layers, and in fact works better as the layers get thicker. This approach could be used in conjunction with CMP to both reduce the number of times CMP is required in a process, and the amount of material removed. For non-optical applications, CMP could be avoided altogether.

Depending on the design, this planarization scheme can involve laborious computer aided design layout of masks. This might often be a worthwhile trade-off, especially if the fabrication is being performed in a foundry process, where it is not possible to add an additional planarization step in the process flow.

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